Student Assistant (m/f/) in cooperation with Fraunhofer AISEC*

Digital Design Engineer for Security Applications

Fraunhofer AISEC and TU Munich are collaborating in designing security chip prototypes for various research projects. You have the opportunity to work with a team of researchers on realizing innovative security solutions on hardware circuits. During your work, you will use state-of-the-art EDA tools, learn valuable skills related to the different stages of chip design and have the opportunity to contribute to cutting edge research. This job is an ideal starting point for a future career in chip design and information security. We also offer Research Internships and Master Thesis positions.

Task Description

Within this work, you will

- Assist implementing and verifying hardware implementations
- Maintain and improve IP cores and tooling
- Document hardware designs
- Evaluate hardware implementations on AMD/Xilinx FPGAs

Requirements

- First experience in hardware design using VHDL or SystemVerilog
- Basic knowledge about FPGA or ASIC design flow
- Good programming skills in Python
- High motivation to learn more about information security and hardware design

Contact

Please send your application with current CV and transcript of records to:

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